Two Methods to Describe New Shift Registers

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ABSTRACT

Shift registers are typical digital logic structures for integrated circuits and are widely used in hardware descriptions. They can be used as early units before memories and be replaced by them later. In multi-precision shift registers, the control signal has heavy loads, and the critical path appears if the input is complex. In this paper, two techniques for synthesis are proposed to reduce either the critical path or power consumption. The first method divides the shift register into 2 or 3 parts, while the second method applies word-based registers to act as the shift register. Both techniques localize the control signals and reduce the path delay.

CCS CONCEPTS

• **Hardware**; • **Communication hardware, interfaces and storage**; • **Buses and high-speed links**;

KEYWORDS

Shift register, Synthesis, FPGA, Critical path

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1 INTRODUCTION

Shift register is a typical structure in integrated circuits and can be applied for regular VLSI architectures. It can be used for the storage, input and output of multi-precision integers. For example, an N-bit integer can be entered in N/w clock cycles, and w bits are entered at each clock cycle. Shift register makes the operation of long-precision integers be operated word by word, which helps parallel-serial conversion and then reduces the drive loads. Besides, it can use scan registers in scan chain to construct shift registers, which improves its speed [1].

Usually, the shift register is built for storage and easy for reading and writing. Compared with RAMs or ROMs, it does not require addresses and can directly receive values. Shift registers can be left-shifted or right-shifted. In general, the shift function in a computer system is fixed by the hardware structure, and the related operations or instructions can be designed. By contrast, the VLSI design the shift register can be generated by gates, and it can also be constructed by IP cores in FPGA or EDA vendors. Some shift register can also be fabricated by advanced Fin-Fet technology process to decrease power consumption [2].

Except the usage as memory units, the shift register can also be used for serial-parallel conversion. It can store irregular big data at first time, and then transfer the data by words. Linear feedback shift register (LFSR) is an important kind for the usage of shift registers. It is frequently used for peudo random number generators. Some coding algorithm also applied LFSR for implementation [3].

In this brief, two architectures are proposed to improve the performance of a shift register and lower down its power consumption. Especially, if the shift register is applied in the situation that the input and output are separated, then the registers in the shift register are not required to shift in the meantime. So it is possible to adjust the input and output logic to bring down the power consumption and reduce the critical paths.

The rest of this paper is organized as follows: Sect. 2 introduces the two methods to describe new shift registers, and Sect. 3 gives the FPGA implementation results. The last Section concludes this paper.

2 TWO METHODS

2.1 Divide into 2 or 3 Shift Registers

As is shown in Figure 1, a shift register can be implemented by two shift registers, where the input and output ports are increased from 1 to 2. Note that the input/output behavior can be kept as before. A regular shift register supports parallel output.

The benefits of the above changes lie at that the control logic of the shift register can be simplified. The two shift registers can be decoded separately so as to decrease the drive loads. Suppose the register $\boldsymbol{R}$ has m words, with word size w, while the registers $\boldsymbol{R}_1$ and $\boldsymbol{R}_2$ both have $m/2$ words. In typical cyclic shift, all the m words in register $\boldsymbol{R}$ need to shift m times, but the m/2 words of $\boldsymbol{R}_0$ only shift $m/2$ times. Also, all the m/2 words of $\boldsymbol{R}_1$ still shift $m/2$ times. As is illustrated in Figure 2, the power cost of the two connected shift registers is about one half of that with the original shift register: $2\cdot (m/2)^2/\mathrm{m}^2 = 1/2$.

In Figure 3, one register is divided into three registers. Its power consumption is about 1/3 of that before division. However, only 1/3 of the registers are shifted during the shift processes.

Figure 4 shows that a shift register is separated into 3 shift registers, whose shift times and numbers are both 1/3 of those before separation. As a result, the total energy for input and output of the shift register is about $(1/3)\cdot 2^3 = 1/3$ of that before. It should be noticed that the control signals for the 3 new shift registers require separate considerations. One may use a counter to count the values of $m/3$, $2m/3$, and m, and provide three control signals.

It should be noticed that the new shift registers is different from the original one in whether the whole register bits or words are required to shift. In the new architecture, only a half or a third of

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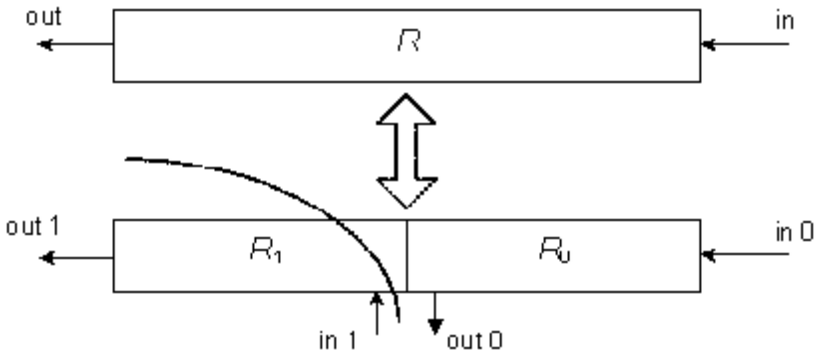

Figure 1: Implement One Shift Register by 2 Shift Registers.

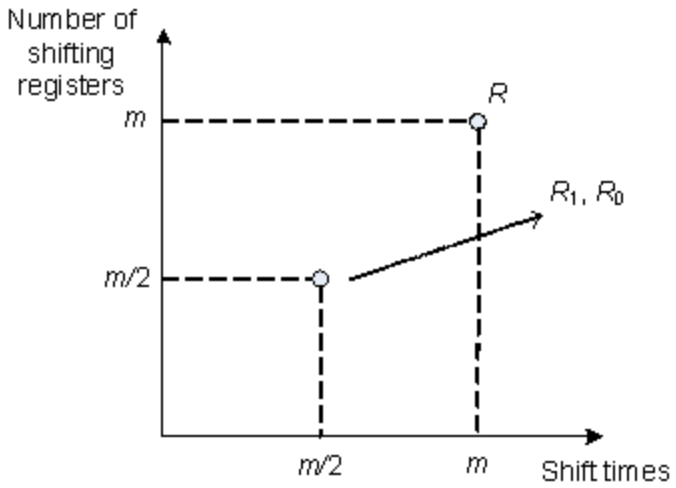

Figure 2: The Division of 1 Shift Register into 2 Shift Registers Brings Down the Energy Consumption by a Half.

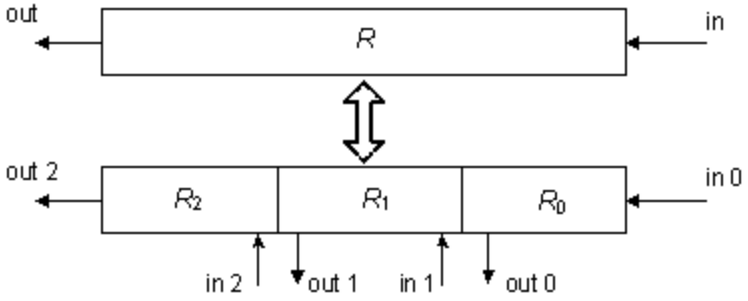

Figure 3: Implement 1 Shift Register by 3 Shift Registers.

the while register words or bits need to shift in the same time. As a result, the control signals are relatively localized. By contrast, all the register bits and words must shift in the meantime, as long as the control signals are stimulated. These control signals force many registers in quite a few long paths and cause apparent time delays, which makes shift registers as critical paths in many logic designs.

2.2 Shift Words in Registers

Figure 5 shows the case of shifting words in registers. The registers are recorded as R_0, R_1, Figure $R_{m\text{-}1}$. In the new approach, $R_{m\text{-}1}$ shifts once, R_1 shifts m-1 times, and R_0 shifts m times.

In the regular shift register there is only 1 control signal, however, the proposal requires m separate control signals for shifting words. Each control signal controls one word of of the shift register. The

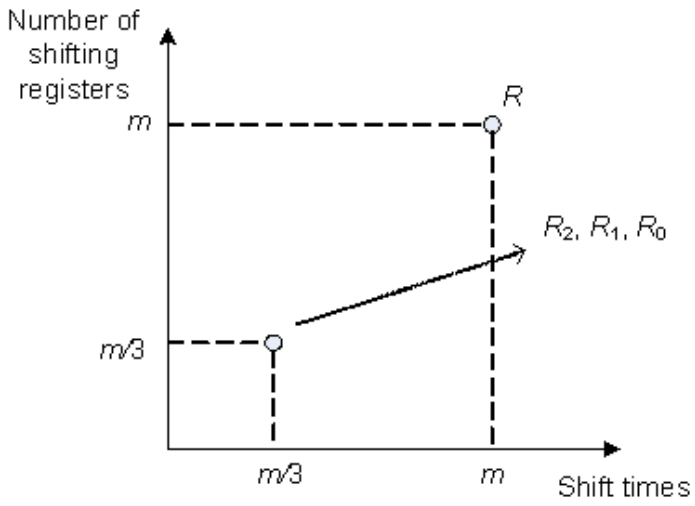

Figure 4: Changes of Shift Register Numbers and Times after Dividing 1 Shift Register into 3 Shift Registers.

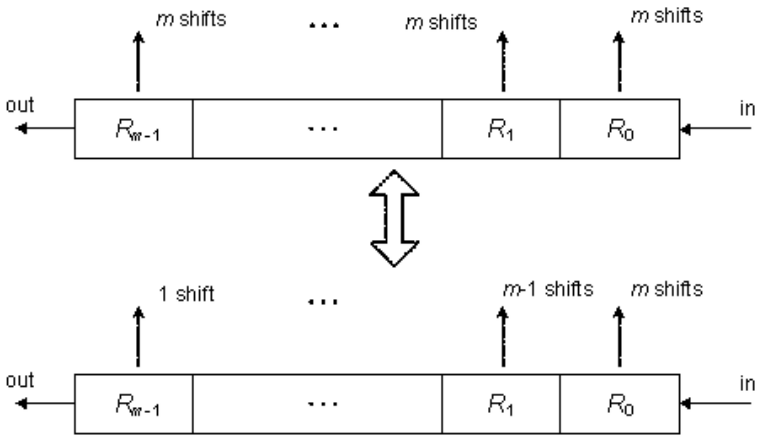

Figure 5: Shift Words in Registers.

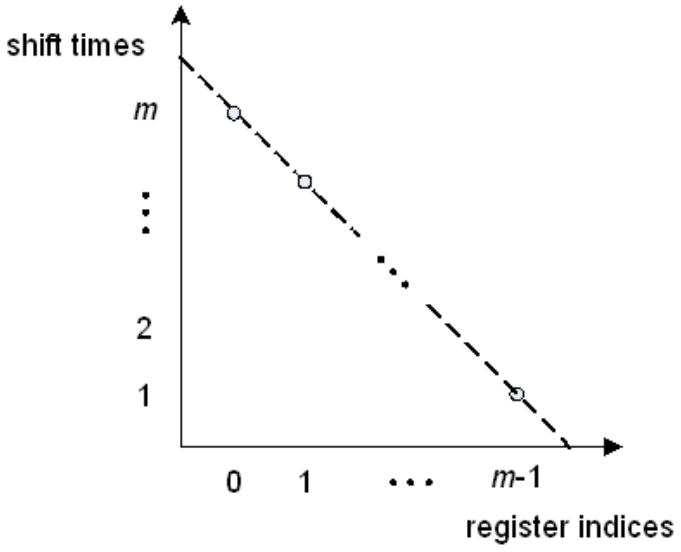

Figure 6: Count the Number of Word Shifts in the Whole Shift Register.

Table 1: Hardware Implementation of N-bit Shift-in and Shift-out Register

Reference	Length (bits)	Technology	Word (bits)	Area 1 (REGs)	Area 2 (LUTs)	f/ Max. f (MHz)	Clk Cycles	Time (μs)	Power (W)
Shift-1	1024	XC7VX330-3	32	135	123/123	400/555.6	66	0.165	0.224/0.242
Shift-2	1024	XC7VX330-3	32	238	245/247	400/666.7	66	0.165	0.208/0.227
Shift-2b	1024	XC7VX330-3	32	303	350/352	400/666.7	66	0.165	0.214/0.238
Shift-3	1024	XC7VX330-3	32	1160	180/181	400/588.2	66	0.165	0.279/0.326

Figure 7: Shift Plan 1: Schematic of Shift Register in Xilinx Vivado.

advantages lie on two points: 1. reduce the drive loads of control signals; 2. decrease the power consumption for shifts.

In Figure 6, in one cyclic shift, the total shift times of all the words are $\sum_{i=1}^{m} i = m(m+1)/2$. By contrast, the original shift registers need to shift m^2 times. Therefore, its total shift times is less than a half of that before, and the power consumption is about 50%.

This structure proposes a minimal cell for every shifting word, so that the control signals are all specialized and localized. Although the area overhead is increased, the critical path is efficiently reduced, which is really useful for complex branches within HDL.

3 FPGA IMPLEMENTATION

Suppose the usual shift register is Plan 1, the division of shift registers into 2 refers to Plan 2, and the word-based shift register is marked with Plan 3. The area overhead with Shift-1 in Plan 1 is smallest, but the critical path is longest which constrains the highest frequency in synthesis. Based upon the synthesis results in Xilinx Vivado 2019, Plan 2 divides the long shift register into 2 smaller shift registers, and the so-called Shift-2 decreases both the critical path delay and the power consumption. Nevertheless the area overhead of the shift register increases. Plan 3 or Shift-3 is composed of m words in registers, in which the power consumption is increased

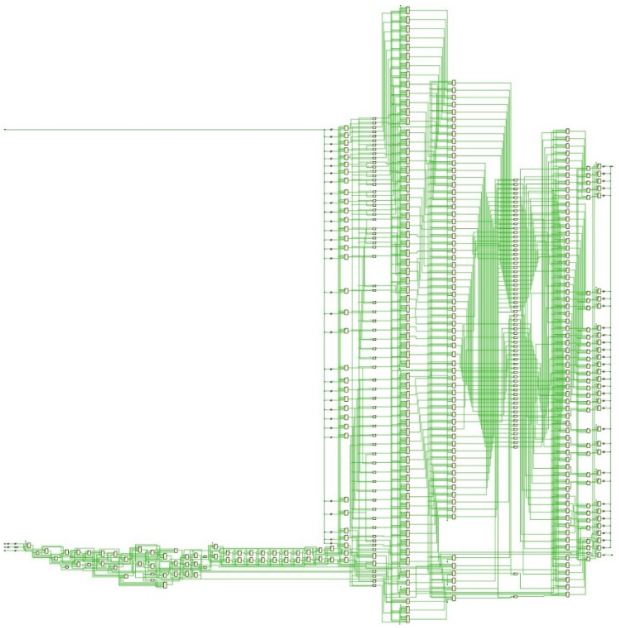

Figure 8: Shift Plan 2- Schematic of Dividing the Shift Register into 2 or 3 Shift Registers in Xilinx Vivado.

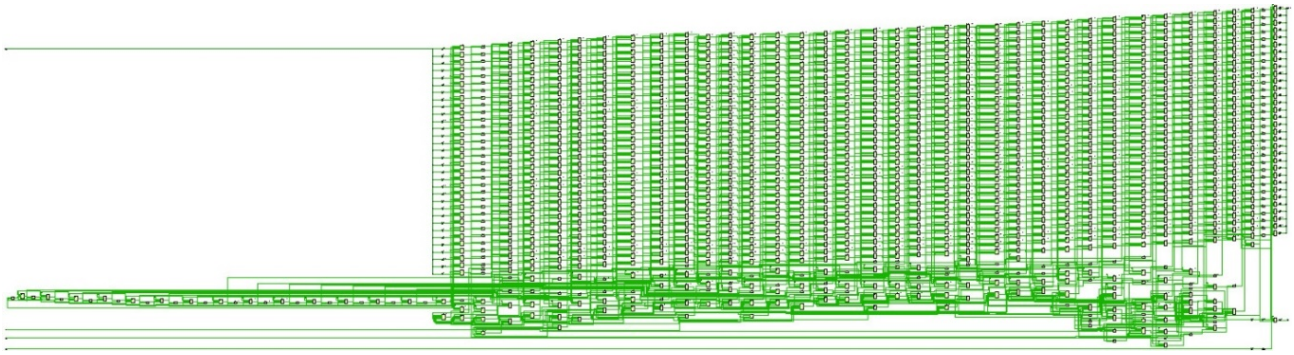

Figure 9: Shift Plan 3—Schematic of Shifting Words in Registers in Xilinx Vivado.

while the critical path is still reduced to some extent. Shift-3 is fit for timing closures. Finally, as is shown in Table 1 the three plans describe 1024-bit shift registers, which needs 66 clock cycles for input and output. Shift-1 refers to general shift register, Shift-2 is divide-by-2 shift register in Figure 1, Shift-2b is divide-by-3 shift register in Figure 3, and Shift-3 refers to shifting words in registers in Figure 5. In Tab. 1, the work frequency f and its maximum Max. f are shown, and the correspondence powers are also demonstrated. It can be found that the maximum frequencies are increased with respect to Shift-1.

Figure 7∼9 refers to 3 schematics with Plan 1∼ Plan 3, in which the yellow squares represent flip-flops or registers. The green lines denote connection wires. It can be found that the three different architectures correspond to different circuits. Plan 2 decreases both the power consumption and the critical path delay. Plan 3 mainly decreases the critical path delay of a shift register.

4 CONCLUSION

Two synthesis plans are proposed to optimize the performance of long shift registers: the first plan is to divide the long shift register into 2∼3 shift registers, and the second one is to shift words in registers. The first method efficiently reduces the power consumption and the drive loads, while the second one mainly reduces the critical paths and improve the maximum frequency.

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